Code No: 861AB

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JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
MCA I Semester Examinations, March - 2023
COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours **Max.Marks:75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, Answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a) What are the four phases in the instruction cycle? [5]
b) What is the role of control address register in control memory? [5]
c) How are alphabets stored in binary form? [5]
d) Show a typical communication link between the processor and several peripherals. [5]
e) Illustrate vector operations on vector processors. [5]

PART – B

(50 Marks)

2. Construct 4-bit arithmetic circuit using full adders, multiplexers and gates. Explain its functionality with the help of function table. [10]

OR

3.a) Explain the eight basic computer registers and their purpose in program execution.
b) With the help of a flowchart explain interrupt cycle. [5+5]

4. Draw a block diagram of a control memory and the associated hardware needed for selecting the next microinstruction address. Explain its working with a suitable instruction. [10]

OR

5.a) Contrast indexed addressing mode with base register addressing mode.
b) Explain various instruction formats. [4+6]

6.a) Make a comparison of n's complement with n-1's complement representations.
b) Discuss IEEE 754 standard for floating point representation. [5+5]

OR

7. Demonstrate Booth's algorithm for multiplication of two signed-2's complement numbers. [10]

8.a) What is FIFO buffer? With the help of a diagram explain the logic of 4X4 FIFO buffer.
b) Discuss cycle stealing in DMA. [6+4]

OR

9.a) Describe the block diagram of associative memory.
b) Differentiate between direct mapping and associative mapping for cache memory. [5+5]

10.a) Explain SIMD array processor with a general block diagram.
b) Illustrate the functioning of arithmetic pipeline. [5+5]

OR

11.a) Discuss the characteristics of multiprocessor systems.
b) Describe the parallel arbitration logic used in multiprocessor system. [5+5]

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